Remarks

Claims 1, 11, 22 and 24 have been amended. Claims 3 and 25 have been canceled. Therefore, claims 1, 4-11, 13-22, 24 and 26-28 are now presented for examination.

In a Final Office Action filed April 25, 2006, claims 1, 4, 5, 10, 11, 22, and 24 stand rejected under 35 U.S.C. §102(e) as being anticipated by Ware et al. (U.S. Pub. No. 2004/0054845). Applicants submit that the present claims are patentable over Ware.

Ware discloses use of slew rate control circuitry and transfer characteristic control circuitry in the pre-driver and driver of transmitter blocks to allow adjustment to different characteristic bus impedances and to allow adjustment for other bus properties, including a calibration process to optimize the circuitry. See Ware at paragraph [0061].

Claim 1 of the present application recites a slew rate detection mechanism to detect a slew rate of an output signal transmitted from an I/O buffer. Applicants submit Ware fails to disclose a chipset having a slew rate detection mechanism that detects a slew rate of an output signal transmitted from an I/O buffer within the chipset. Consequently, claim 1 is patentable over Ware. Claims 4-10 depend from claim 1 and include additional features. Therefore, claims 4-10 are also patentable over Ware.

Claim 11 recites a slew rate detection mechanism to detect a slew rate of an output signal transmitted from an I/O buffer. For the reasons described above with respect to claim 1, claim 11 is also patentable over Ware. Because claims 13-17 depend from claim 11 and include additional features. Therefore, claims 13-17 are also patentable over Ware.

Claim 18 recites receiving a signal at a slew rate detection mechanism within a chipset via a bus. For the reasons described above with respect to claim 1, claim 18 is

also patentable over Ware. Since claims 19-21 depend from claim 18 and include additional features. Therefore, claims 19-21 are also patentable over Ware.

Claim 22 recites a slew rate detection mechanism to detect the slew rate of an output signal transmitted from an I/O buffer. Thus, for reasons described above with respect to claim 1, claim 22 is also patentable over Ware. Because claims 24 and 26-28 depend from claim 22 and include additional features. Therefore, claims 24 and 26-28 are also patentable over Ware.

Claims 3, 18, 21 and 25 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Ware and Donnelly et al. (U.S. Patent No. 5,959,481). Applicants submit that the present claims are patentable over Ware even in view of Donnelly.

Donnelly discloses a bus driver circuit having slew rate control. The bus driver circuit includes a first circuit having an input configured to receive a data signal and an output operative to output a drive signal in response to the data signal, Further, the circuit includes a second circuit coupled in parallel with the first circuit and operative to receive a slew rate control signal and a slew rate indicator circuit coupled to the second circuit. See Donnelly at Abstract. The slew rate indicator circuit is a process-voltage-temperature or "PVT" detector circuit that indicates whether variations in the fabrication process (e.g., transistor dimensions, dielectric dimensions, thresholds, gain, etc.), supply voltage, input voltage, or operating temperature result in variations in the slew rate of DRIVE or OUT signals of the bus driver circuit. If the slew rate indicator indicates that variations in operating or PVT conditions would otherwise cause the slew rate of the DRIVE or OUT signal to be too slow, the slew rate indicator causes an SRCTL signal to enable a three-state inverter. If the slew rate indicator indicates that operating or PVT

conditions may cause the slew rate of the DRIVE or OUT signal to be equal to or faster than the nominal slew rate, the slew rate indicator causes the SRCTL signal to disable the three-state inverter (col. 4, ll. 44-65).

Nevertheless, Donnelly does not disclose or suggest a slew rate detection mechanism to detect a slew rate of an output signal transmitted from an I/O buffer as recited in the present claims. Instead, Donnelly discloses a slew rate indicator circuit that detects PVT conditions that indicate variations in the slew rate of output signals of the bus driver circuit. Applicants submit that *a slew rate indicator circuit that* ***detects PVT conditions*** *is not equivalent to the claimed slew rate detection mechanism that* ***detects a slew rate of an output signal transmitted from an I/O buffer.***

As discussed above, Ware does not disclose or suggest a slew rate detection mechanism that detects the slew rate of an output signal transmitted from an I/O buffer. Thus, any combination of Ware and Donnelly would also not disclose or suggest a slew rate detection mechanism that detects the slew rate of an output signal transmitted from an I/O buffer. Accordingly, the present claims are patentable over Ware in view of Donnelly.

Claims 6, 9, 15 and 26 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Ware and Donnelly, and further in view of Lee et al. (U.S. Patent No. 6,614,285). Applicants submit that the present claims are patentable over a combination of Ware, Donnelly and Lee.

Lee discloses power available to an integrator circuit being controlled so that relatively high power is provided during one phase of operation, such as during an interval when slewing in a device is expected and relatively low power is provided during

another phase. See Lee at Abstract. However, Lee does not disclose or suggest a slew rate detection mechanism that detects the slew rate of an output signal transmitted from an I/O buffer.

As discussed above, Ware and Donnelly both fail to disclose or suggest a slew rate detection mechanism that detects the slew rate of an output signal transmitted from an I/O buffer. Therefore, any combination of Ware, Donnelly and Lee would also not disclose or suggest a slew rate detection mechanism that detects the slew rate of an output signal transmitted from an I/O buffer. Therefore, the present claims are patentable over the combination of Ware, Donnelly and Lee.

Claims 7, 8, 16, 17, 19, 20, 27 and 28 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Ware, Donnelly and Lee and further in view of Namiki (U.S. Patent No. 4,704,642). Applicants submit that the present claims are patentable over a combination of Ware, Donnelly, Lee and Namiki.

Namiki discloses a noise reduction circuit provided with a slew rate detection circuit for detecting a slew rate of a reproduced audio signal, and variably controls a pulse width of a hold signal depending on the detected slew rate. See Namiki at Abstract. Nonetheless, Namiki does not disclose or suggest a slew rate detection mechanism that detects the slew rate of an output signal transmitted from an I/O buffer.

As discussed above, Ware, Donnelly and Lee do not to disclose or suggest such a feature. Thus, any combination of Ware, Donnelly and Lee would also not disclose or the feature. Consequently, the present claims are patentable over the combination of Ware, Donnelly, Lee and Namiki.

Applicants respectfully submit that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,
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